# DECCA

# D20TFG5

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## Section 1 SAFETY AND ISOLATION

1) Under no circumstances should any form of repair or maintenance be attempted by any person other than a competent technician or engineer. The following precautions should be observed:
2) For purposes of servicing, the chassis should be supplied from an isolation transformer of at least 150W rating.
3) If disturbed, the original lead dressing should be restored. This is particularly important due to the 'hot coil' nature of the chassis. Lead dressing will also have a bearing on the EMC performance of the chassis.
4) Components marked ⚠ on the circuit diagram are safety approved types and have special safety related characteristics. Only the manufacturers replacement components should be used. Replacement with alternative or 'up-rated' parts e.g. higher power resistors definitely does not guarantee the same level of protection and may create a fire, electric shock or X-radiation hazard.
5) Components not bearing the ⚠ mark should still be replaced with the originally fitted type and should be mounted in the same way.

### 1.1 The Isolation Barrier

The chassis is a 'hot-coil' chassis whereby the line deflection coils are NOT isolated from the mains since the PSU does not provide B+ rail isolation. Consequently, the mains isolation barrier is more convoluted than in a conventional chassis and a much larger portion of the chassis is non-isolated. Figure 1 shows the isolation barrier position in the chassis.

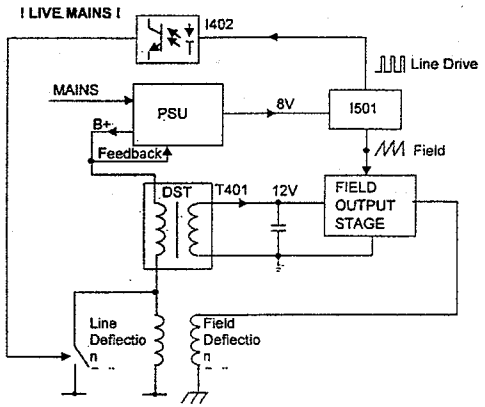



Fig 1 **Mains Isolation Barrier Positions**

It can be seen that both the DST (T401) and the scan coils now straddle the isolation barrier and are, as such, safety critical components. Also, the opto-coupler (I402) is required to pass line drive from I501 on the 'cold' side to the line drive stage on the 'hot' side. The isolation barrier therefore consists of T802, T401, I402, C804, R804, R805, the scan coils and 6mm air gaps. To maintain barrier integrity care should be taken not to reduce any air gaps, e.g. by protruding wires, following component replacement.

Deflection yoke lead dressing is important to maintain double insulation across the isolation barrier. The position of the deflection lead sleeving is maintained by a tie wrap. Should this be removed for any reason, the sleeving should be slid towards the deflection yoke and tie wrapped into position.

### 1.2 Semiconductor Device Handling Precautions

The chassis contains devices which may be damaged by static electrical charge during handling, particularly I501, I602, I701 and Q801. To avoid damage, soldering irons should be earthed and service engineers should ideally wear wrist straps earthed through a 1M resistor or at least discharge themselves to an earthed point.

## Section 2 SWITCHED MODE POWER SUPPLY

### 2.1 Summary

The power supply is a self-oscillating discontinuous buck converter under peak current control and designed for up to 65W output power at nominally 98V. The main B+ output of this converter topology is inherently non-isolated and as such, output voltage feedback does not require an opto-coupler. Some energy is derived in flyback mode via an isolated winding on the buck inductor to provide a low power 10V secondary supply from which are derived switched 8V (video processor) and permanent 5V (µP) supplies.

In stand-by mode, both the B+ and 10V supplies remain close to their nominal operating levels but with virtually zero load, the PSU enters a burst-mode whereby typically 180 in 200 cycles are skipped. In this way, the stand-by power consumption (including degaussing circuit) is less than 4W.

### 2.2 Description of Operation of the Buck Converter

Figure 2 shows the main components of the buck converter. The output voltage may be controlled between zero and the input voltage by varying the on-time of Q801. During this period, Vin-Vout is applied across the buck inductor (T802 winding pins 7 & 8) and the current in it ramps up linearly. When Q801 is turned off, -Vout is applied across the buck inductor and energy is delivered to the load and C809 combination.

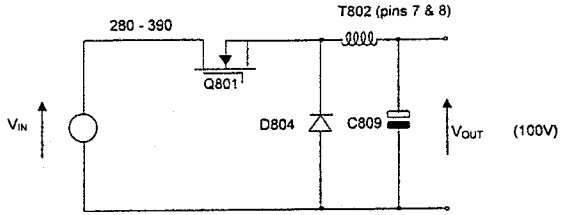



Fig 2 **The Buck Converter Topology**

### 2.3 Start-Up

At start-up, the overwind output voltage (T802 winding pins 7 & 8) is not present so a start-up bias circuit is required. This consists of R806, D802 and R809. Approximately 16V is produced at the junction of R806 and D802 which is fed via R809 to turn on Q801 for the first time.

### 2.4 Control Method

During the on-time of Q801, the buck inductor voltage flows through the current sense resistor R814 forming an analogue of the buck inductor current. This is fed to the base of Q802 along with a DC bias current from the error amplifier (via R813) such that once a certain buck inductor current level is reached, Q802 turns on. When this happens Q801 is turned off and the the inductor current free-wheels through D804. This is peak current-mode control.



### 2.5 Output Voltage Regulation

The non-isolated B+ rail means that no opto-isolator is required for direct Vo control. It can be seen from Figure 3 that Vo minus a small zener voltage drives the emitter of this transistor (Vo-Vz) whilst a resistive potential divider feeds the base (kVo, k<1). If, for instance, the output voltage tends to rise, Ve rises by ΔVo whereas Vb only rises by ΔkVo. The net result is an increase in negative bias and an increase in collector (control) current. R818 in the potential divider provides an element of control over the B+ voltage.

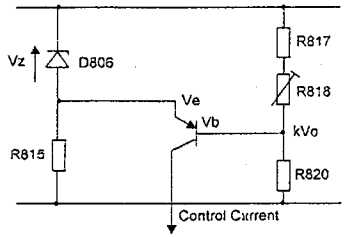



Fig 3 **The Error Amplifier**

### 2.6 Overvoltage Protection

If the power switch Q801 should become short-circuit, the full rectified mains voltage appears at the output which would over stress components in both the PSU itself and the load. In order to limit the output voltage rise under these conditions, a 130V 5W zener diode D805 is fitted across the B+ output. An over-voltage causes conduction of D805, shorting the B+ output and blowing the fuse F801.

### 2.7 Isolated Supplies

In order to provide low voltage isolated supplies, a secondary winding is included on the buck inductor, phased such that energy is delivered in flyback mode, that is when Q801 is off. During this interval, the buck inductor voltage is clamped to the output voltage and the turns ratio is chosen to provide a secondary of 10V with rectification and smoothing performed by D807 and C812 and overload protection by R821. A permanent 5V µP supply is derived from this 10V supply by I801 as well as an 8V switched supply under µP control by Q804, R822, D808 and Q805.

### 2.8 Chassis Start-Up Procedure

The PSU topology used in the chassis has a characteristic which complicates start-up. Until a B+ load is established (i.e. the line output stage starts), the isolated secondaries are very high impedance - simply turning on the video processor 8V supply and waiting for line-drive to start-up would fail since the supply cannot deliver I501's supply current. In order to overcome this problem, a system of 'pseudo line-drive' was devised which allows the line output stage to be driven by the µP in order to establish a B+ load prior to turn-on of the video processor 8V supply. Figure 4 is a block representation of this system.

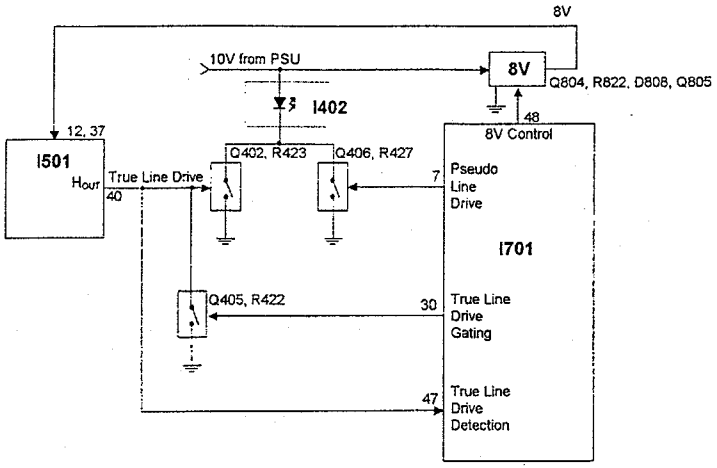



Fig 4 **Start-up Circuit Block Diagram**

The two line drive sources are connected together at the input of I402. The two driver transistors, Q402 and Q406 acting as an OR-gate. The µP is responsible for ensuring that both line drive sources cannot drive the output stage simultaneously and to achieve this, the true line drive from I501 is monitored (µP pin 47). In this way, the transition from pseudo to true line-drive is timed to the latter starting up. However, the line-drive stage does not reliably operate at 31kHz so the soft-start cycle of I501 must be gated out. The µP achieves this by keeping Q405 on for a fixed time after true line-drive has been detected thus keeping Q402 off. When this time has elapsed, pseudo line-drive is stopped and Q405 turned off simultaneously, completing the start-up sequence.

On reverting to stand-by pin 7 reverts to the high state which maintains I402 in conduction via Q406. This maintains Q403 on and the line output transistor (Q404) off.



# Section 3 TUNER AND IF STAGES

## 3.1 Tuner

The main chassis is fitted with a voltage synthesis Full Band Tuner (for system BG) or UHF tuner (for system I). Control of the tuned frequency is achieved by a voltage on pin 2 of the tuner. This voltage is derived from integrating a 33 volt PWM switched waveform. This PWM waveform is derived from pin 1 of the microcontroller I701.

The AFC is sampled by the microcontroller via the I²C bus from I501 and frequency correction is achieved by microcontroller adjustment of the duty cycle of the PWM which then modifies the tuner frequency.

## 3.2 AGC Adjustment

For most aerial input signal levels the tuner operates at maximum gain. At high signal levels the gain of the tuner is reduced by an AGC voltage generated in the IF stage. The AGC output from the IF (pin 54 of I501) is applied to pin 1 of the tuner (H001).

The AGC maintains a maximum IF voltage of 600mV peak to peak. The voltage level can be adjusted using the following procedure:

Short circuit pins 2 and 3 of P701 to enter service mode. When in service mode use the programme up and down keys to select service parameter 13. Using a 40MHz or greater oscilloscope, monitor pin 11 of TU001. Adjust service parameter 13 using the volume up and down keys for 600mV on pin 11 for a single ended tuner, and 300mV for a differential output tuner. Press the TV key to store the AGC value.

## 3.3 Vision Decoding

The majority of the vision and sound, deflection and colour decoding is performed by I501. The IF signal passes from the tuner through the SAW filter (X001) to filter unwanted frequencies to I501. It is demodulated internally and the output at pin 6 is buffered by Q501. The sound and vision components are now separated. Z501 removes the sound from the vision components and Z601/602 filters the FM sound to pin 1 for demodulation. Video is then fed to the SCART socket output, pin 19 of P501 via Q502.

## Section 4 SOURCE SELECTION

### 4.1 RGB

Source selection is controlled by the microcontroller via I²C bus commands. The video processor I501 can select between internal demodulated CVBS video on its pin 13, external CVBS video (AV1) from pin 20 of P501 on its pin 17 or, if available, from external CVBS video (AV2) from the yellow phono socket of PA501, which is applied to pin 11. The internally demodulated CVBS video is always available on pin 19 of P501.

External RGB is selected within I501. Fast blanking pulses from pin 16 of P501 are passed via an OR-gate circuit of Q301-304 and associated components to pin 26 of I501. This pin controls the state of the RGB outputs to the tube base pins 19, 20 and 21. It has three possible states:

| | | |
|---|---|---|
| 1) | Less than 0.4V | Internal RGB from colour decoder. |
| 2) | Between 0.4V and 4.0V | External RGB from pins 7, 11 and 15. |
| 3) | Greater than 4V | Output blanked for OSD/Text insertion. |

When teletext or OSD is displayed, pin 35 of I703 goes from ground to 5.0 Volts. This signal is passed via Q301 and causes pin 26 of I501 to enter the third state above, independent of the state of the other inputs to the OR-gate circuit. During mixed TV/Text mode or whilst the OSD is showing on part of the screen this line will be switching at a high rate. RGB mode can be selected manually by the user and in this case the open-drain output on pin 8 of the micro-controller will be switched off and will be pulled up to 1.7 volts by R307 and R306. Q302 then applies a voltage of about 1.0 volts to pin 26 of I501. In the absence of a higher voltage via Q301 and Q303 from the fast blanking input, pin 16 of P501, this is still sufficient to enter the external RGB mode.

### 4.2 Audio

Audio source switching is controlled via the microprocessor I701. The audio is switched from internal to external source via I²C in I501. Internal source is fed to I501 at pin 1 and the external source at pin 2. On models equipped with front AV, the external source is provided either from pins 2 and 6 of P501 or the white phono socket PA501.The external source selection is controlled by pin 3 of I701 and Q703, then switched by I602. On models without front AV, I602 is omitted and bypassed via R601. On models equipped with a headphone socket, the speaker feed from the audio amplifier (I601) is diverted to the headphone when a headphone jack is plugged into PA601

### 4.3 AV switching

Inputs from pins 8 and 16 of SCART 1 are sampled by analogue to digital conversion on pins 9 and 10 of I701 respectively. The input levels are adjusted such that the controller will automatically switch to AV1 when pin 8 is above 6V and RGB when pin 16 is above 1V. The time constant on pin 16 ensures the controller will not detect real-time RGB insertion using pin 16.

## Section 5 COLOUR DECODER

The luma signal processing and colour decoding are implemented by I501. The luminance and chrominance signals are separated internally. A delay line is also incorporated to compensate for the difference between the luma and chroma processing times. There are no adjustments required on the colour decoder.



## Section 6 HORIZONTAL AND VERTICAL DEFLECTION

In addition to decoding and switching, I501 provides deflection processing for the horizontal and vertical time-base circuits. Using video from the IF or external source as appropriate, the timebase circuit of I501 produces horizontal drive pulses at pin 40 to switch horizontal drive transistor Q402, and a differential vertical ramp at pins 46 and 47 to drive the vertical deflection output amplifier (I401).

All geometry adjustments are performed via the I²C bus with the service parameters (see section 10.2) with the exceptions of picture width (which is fine tuned by adjusting the B+ voltage by means of R818) and horizontal linearity (which is fixed by L402.)

## Section 7 TUBE BASE PANEL

The picture tube amplifiers produce high voltage CRT electrode drives from the low voltage RGB outputs of the TDA884x (I501). They also produce black current information to maintain the grey-scale characteristics which is returned to the colour decoder (I501). Also included is circuitry for picture blanking during switch on.

The picture tube aquadag, (P901), is used to provide beam current information for the colour decoder for the purposes of beam current limiting. The tubebase socket (P902) is fitted with internal spark gaps. D910 provides tube base protection when the spark gaps flash-over.
The panel includes supplies to the tube electrodes and the video amplifiers. Focus and A1 supplies are connected directly from the flying leads of T401.

### 7.1 Video Drives

All video drive adjustments are done via the I²C bus (see section 10.) with the exception of the black level set point (140V) which is set by the A1 control on the FBT (T401). An additional feature for diagnostic purposes is the ability to disable the auto black level circuit by pressing '2' on the remote control hand set when in service parameter 02 (see section 10)

### Tubebase Video Amplifier Circuit

Each video amplifier channel includes a bipolar cascode amplifier. A R, G or B signal from the colour decoder (I501) is fed to each video amplifier input.
The low frequency gain of each video amplifier is approximately 51, this being determined by the ratio of the feedback resistors to the input resistors. The gain of each video amplifier channel above 2.2 MHz is increased by including a small capacitor across one of the two input resistors of each channel.

### 7.3 Video Amplifier Switch-On Blanking

The emitters of Q906, Q907 and Q908 are biased from the +200V video HT via R917, R905 and Q910. The +13V supply to bias the base connections of Q902, Q905 and Q908 is switched on under control from microcontroller I701 pin 35 (via R435, Q408 and R434 on the main panel) during power up or from standby after emitter bias of Q906, Q907 and Q908 is established.
Thus picture blanking during power up or from standby is ensured.

### 7.4 Auto Grey Scale

During the field blanking period the colour decoder (I501) measures the total cathode circuit leakage currents at the video amplifier outputs via Q901, Q902 and Q903. During field blanking, the colour decoder applies monitoring pulses to the video amplifier inputs and thence current outputs from Q901, Q902, Q903 are applied to the colour decoder pin 18 via R904 and R516. (During normal unblanked picture operation, the colour decoder ignores the information on its pin 18.). The current outputs from Q901, Q902 and Q903 are used by I501 to adjust the black current and video gain of each video channel automatically. Thus black level picture beam current and black to white video drives are maintained. Diodes D903, D905 and D906 prevent horizontal smearing/ shadowing of the OSD from spreading across the screen.
For diagnostic purposes this control loop may be disabled by selecting service parameter 02 (hue) and pressing the number 2 key on the hand unit. After repair, the auto black level sampling should always be re-enabled by pressing the number 2 key again and storing it with the TV key. (The value of parameter 02 toggles between two values when the number 2 key is pressed, the lower of which indicates black level sampling is enabled.)



## Section 8 REMOTE CONTROL

### 8.1 Infra-red Transmitter

The hand unit is controlled by IC781, type PCA84C122AT/093, surface mounted on the keypad side of the PCB. When replacing the part, the /093 is significant as it determines the key codes transmitted. Two AA type batteries in series provide a 3V power supply.

The IC remains in standby mode (oscillator not running) until a key on the matrix is pressed. The oscillator, governed by a 4MHz ceramic resonator XL781 is started. The IC decodes the key with suitable debounce and then transmits the relevant code, repeating until the key is released.
The pulse train output is modulated within the IC onto a 33.33kHz (f.osc/120) carrier with low (1:3) hark:space ratio, reducing power consumption and allowing higher LED current. The output on pin 21 of IC781 drives TR781 which provides high current pulses through infra-red transmitter diode D781.

### 8.2 Infra-red Receiver

The chassis uses an integrated receiver, IC702, which provides a fully demodulated output to the microcontroller through R703, pulled up by R702.

| *Keypad N°* | *Symbol* | *Functions* | *Keypad N°* | *Symbol* | *Functions* |
|---|---|---|---|---|---|
| 1 | | Standby | 16 | | Programme Up |
| 2 | 1 | N° 1 | 17 | | Increase Volume |
| 3 | 2 | N° 2 | 18 | | Decrease Volume |
| 4 | 3 | N° 3 | 19 | | *Fastext (RED) |
| 5 | 4 | N° 4 | 20 | | Menu/*Fastext (GREEN) |
| 6 | 5 | N° 5 | 21 | | Menu/*Fastext YELLOW) |
| 7 | 6 | N° 6 | 22 | | Menu/*Fastext (CYAN) |
| 8 | 7 | N° 7 | 23 | | Normalize/*Hold |
| 9 | 8 | N° 8 | 24 | | *Expand |
| 10 | 9 | N° 9 | 25 | | *Reveal |
| 11 | 0 | N° 0 | 26 | | Status/*Fastext Index |
| 12 | | TV | 27 | | AV Select |
| 13 | | *Text/*Mix | 28 | | *Time/*Subcode |
| 14 | | Programme Down | 29 | | Not used |
| 15 | | Mute | 30 | | *Update |

* These functions are only present on chassis fitted with teletext

Table 1 **Keypad Idents and Functions**

## 10.11 Adjustment Locations (Physical )

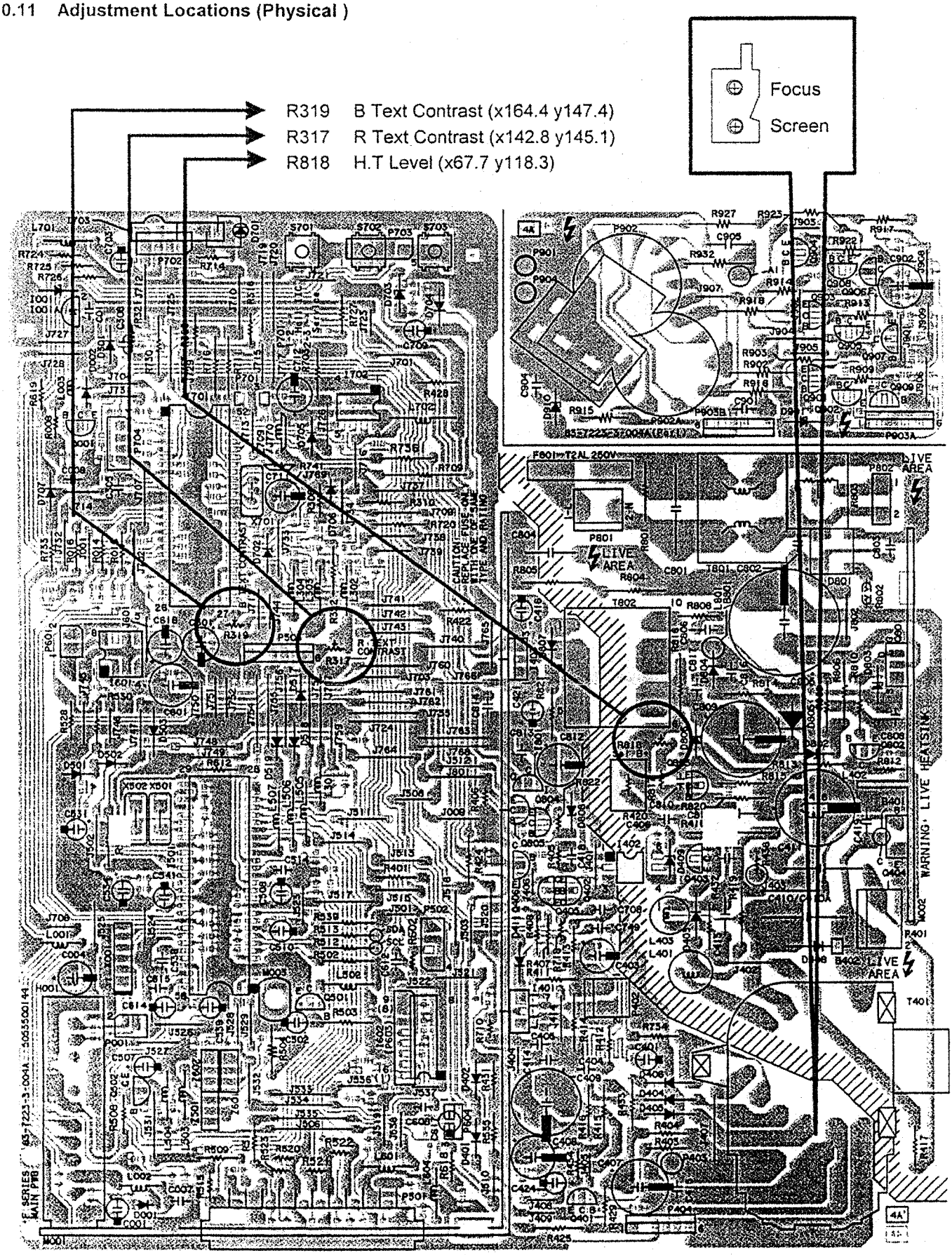
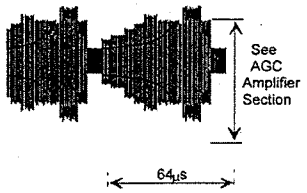



Fig 5 **Adjustment Locations (Main Chassis)**

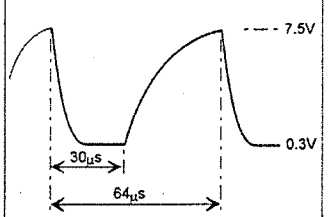
## Section 11 WAVEFORMS

101



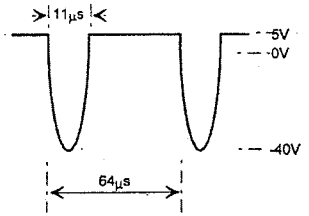

I I. F. INPUT (X001 pin 2)

401



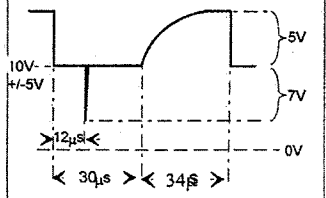

Q402 COLLECTOR

402



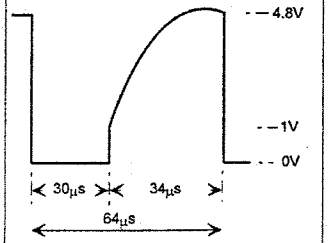

T401 pin 3
Relative to 'hot earth' (PSU heat sink)

403



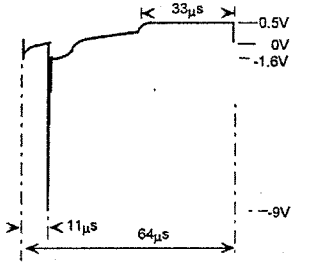

D409 CATHODE relative to 'hot earth'
(PSU heatsink)

404



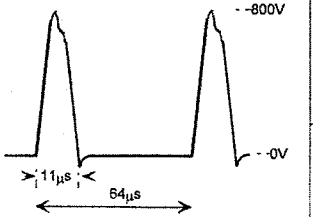

Q403 COLLECTOR relative to 'hot earth'
(PSU heat sink)

405



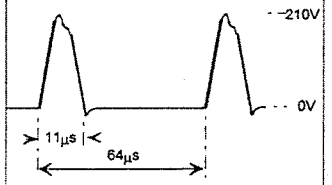

Q404 BASE relative to 'hot earth'
(PSU heat sink)

406



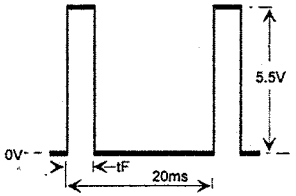

Q404 COLLECTOR relative to 'hot earth'
(PSU heat sink)

407




LINE FLYBACK PULSE (D406 Anode)

408

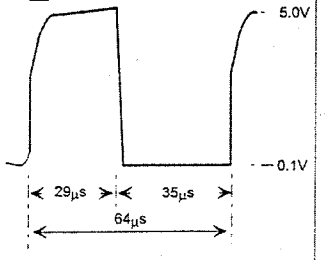



VERTICAL GUARD PULSE
(tF is between 0.5ms and 1.0ms)
(D402 Anode)

409

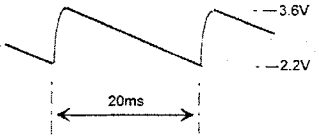
FIELD OUTPUT (Flyback time, tF is between
0.5ms and 1.0ms) At I401 pin 5

501




LINE DRIVE PULSE (I501 pin 40)

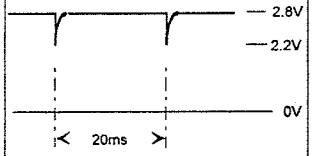
502




FIELD AMPLIFIER DRIVE (I501 pin 46)

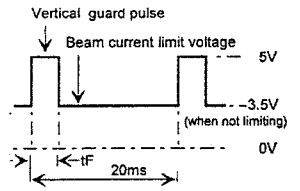


503



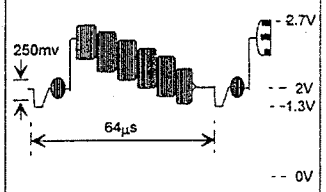

FIELD AMPLIFIER DRIVE REFERENCE
(I501 pin 47)

504



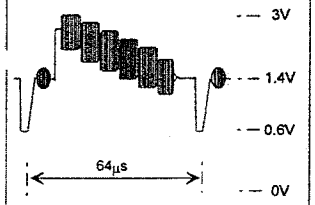

BEAM CURRENT LIMIT/VERTICAL GUARD
(tF is between 0.5ms and 1.0ms in length)
At I501 pin 22

505



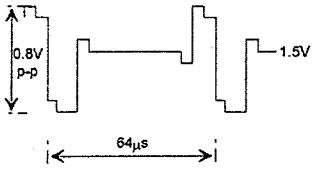

COMPOSITE VIDEO at Q501 Emitter

506



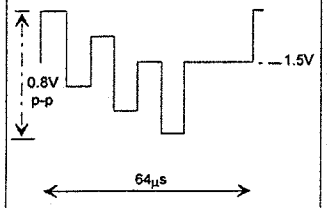

COMPOSITE VIDEO at Q502 Emitter

507



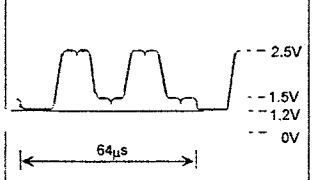

(R-Y) SIGNAL at I501 pins 30 and 32

508



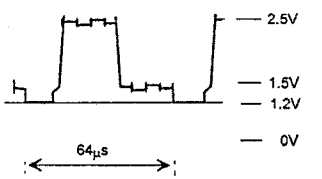

(B-Y) SIGNAL at I501 pins 29 and 31

509



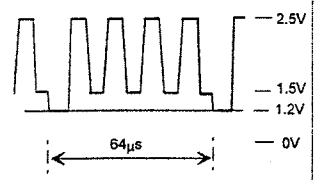

RED VIDEO DRIVE (I501 pin 21)

510



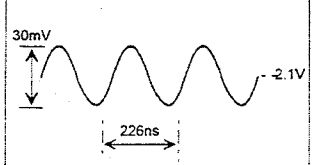

GREEN VIDEO DRIVE (I501 pin 20)

511



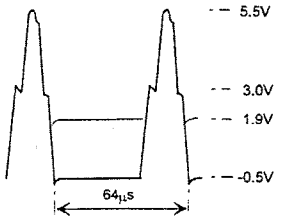

BLUE VIDEO DRIVE (I501 pin 19)

512



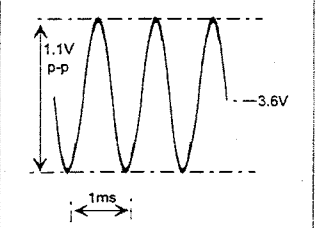

4.43MHz OSCILLATOR (I501 pin 35)

513

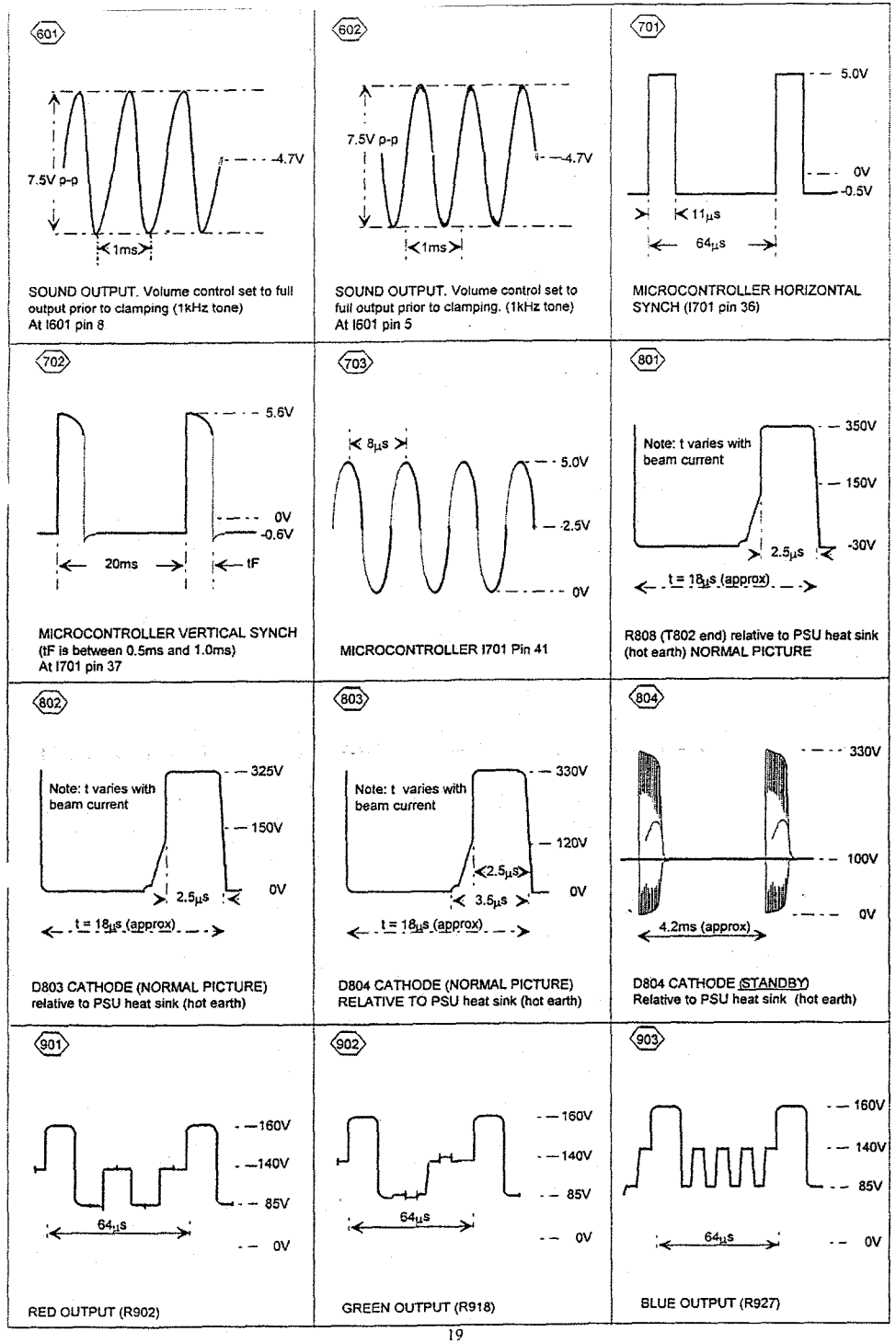



SANDCASTLE PULSE (I501 pin 41)

514




AUDIO OUT (volume control set to
full prior to clamping) at I501 pin 15






# Section 13 CIRCUIT DIAGRAMS

## 13.1 Circuit Diagrams for AV2 PCB

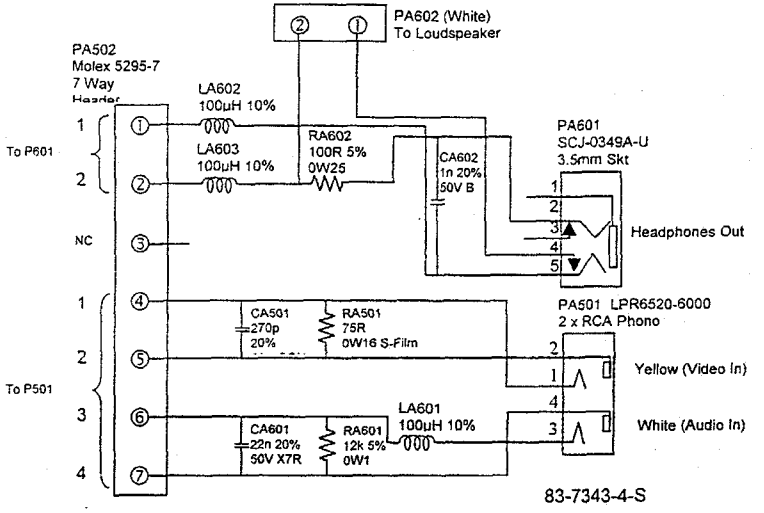



Fig 6 **14" Models**

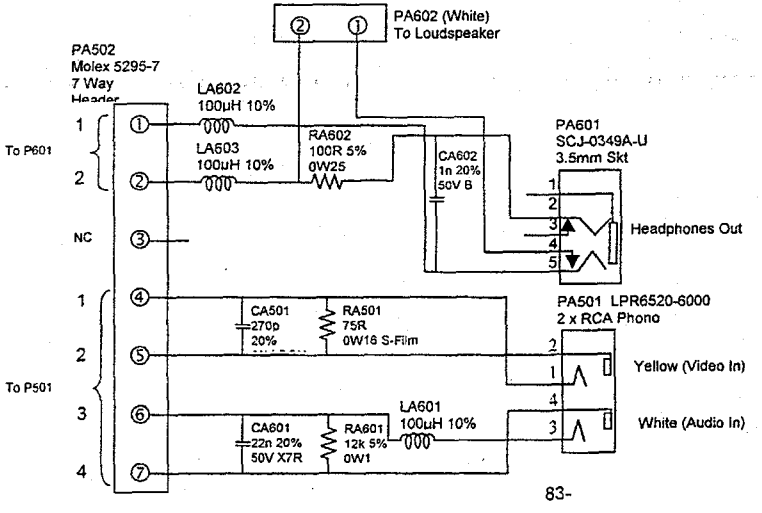
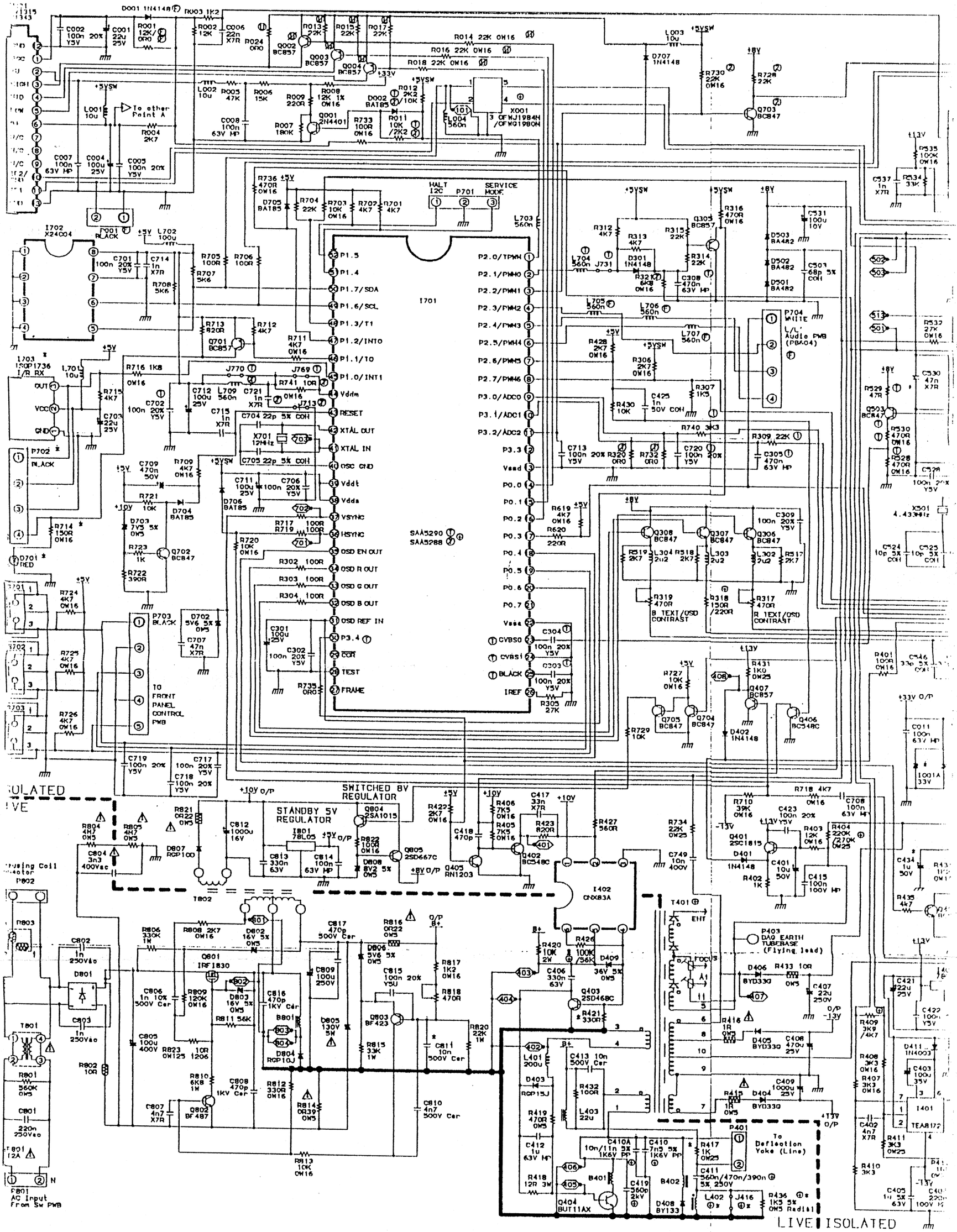



Fig 7 **20" and 21" Models**


SWITCHED 8V REGULATOR
STANDBY 5V REGULATOR
LIVE
ISOLATED
To other Point A
TO FRONT PANEL CONTROL PWB
To Deflection Yoke (Line)
AC Input From Sw PWB
L/L' Audio PWB (PBA04)
HALT I2C
SERVICE MODE
SAA5290
SAA5288
I701
P701
P702
P703
P704
P401
P402
P403
T401
T801
T802
I402
X001
X501
Q404 BUT11AX
Q405 RN1203
Q407 BC857
Q408 BC548C
Q409 BC847
Q410 BC847
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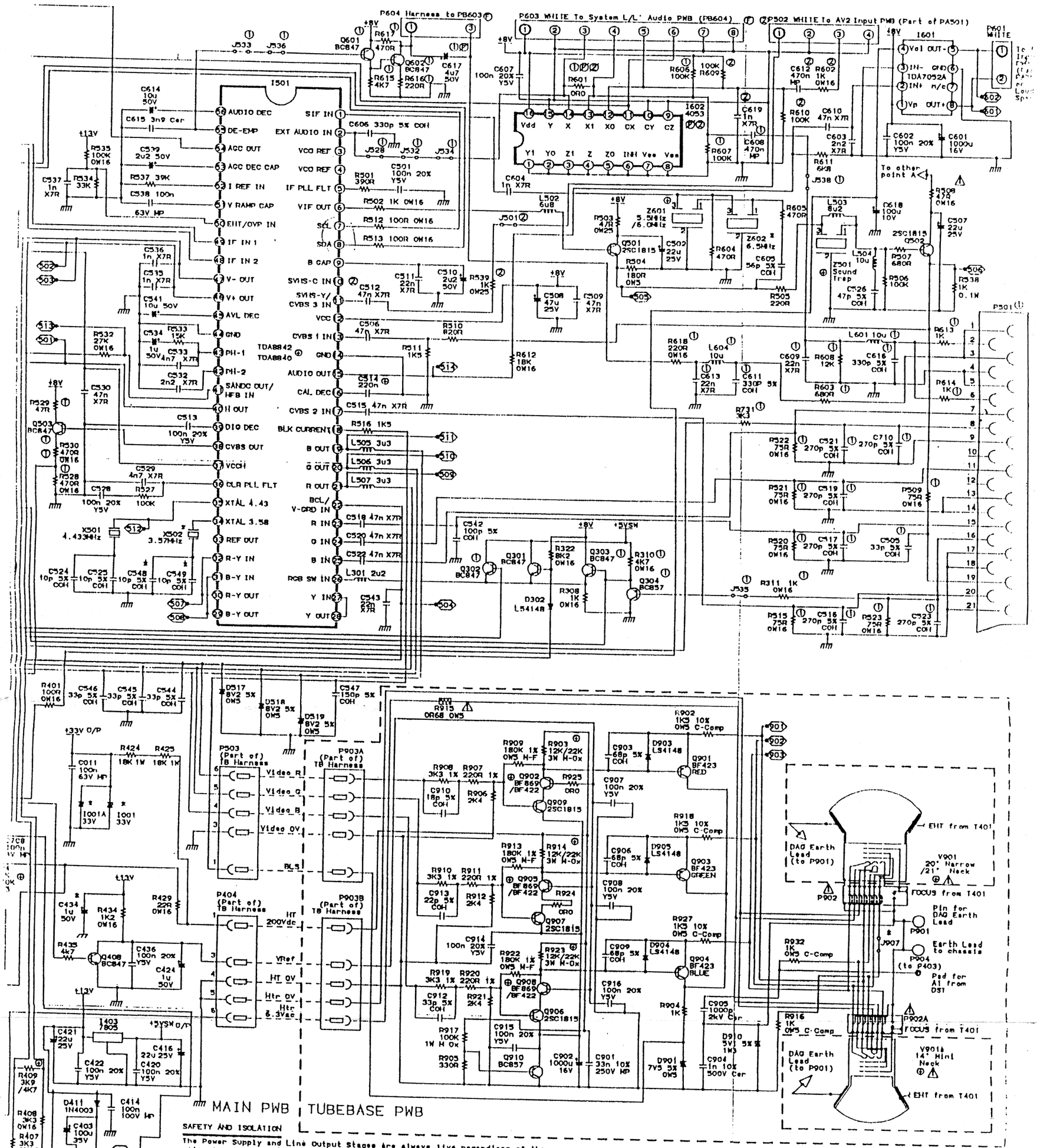


SAFETY AND ISOLATION

The Power Supply and Line Output Stages are always live regardless of the mains supply polarity, therefore, when servicing, the receiver should be supplied through a mains isolation transformer.

The power supply remains charged for approximately 30 seconds after switching off - avoid touching this and the Line Output stage in that time.

Most of the receiver, other than the Power Supply and Line Output stage, is isolated from the mains by: T401; T402; T802; R804 & R805; C804 and an air gap of 6mm or more built into the Chassis and Deflection Yoke. To maintain safety ensure that after repair the air gaps are not reduced by protruding wires etc. Components marked ⚠ in the parts list or on the circuit are 'Approved' types and should be replaced ONLY with components supplied or approved by our Service Department. It is recommended that other replaced parts should be of the type originally fitted, particularly resistors stood off the printed circuit board.

FAILURE TO OBSERVE THE ABOVE MAY RENDER THE CHASSIS AND/OR EXTERNAL PARTS LIVE, OR CAUSE OTHER HAZARDS.

KEY:

- (xxx) Waveform number xxx (dot id 4v4)
- ⁂ May NOT be fitted
- ⊕ Varies between Models
- Ⓕ Fitted on System L/L' Models
- Ⓤ Fitted on UHF Only Models
- ② Fitted on AV2 Equipped Models
- ① Fitted on AV Equipped Models
- Ⓣ Fitted on Teletext models

(Option with '/' indicates opposite)

F Series CTV
Main & Tubebase PWBs

| 83-7223-3-S | | | |
|---|---|---|---|
| DRAWN | ISSUE | DATE | CHK'D |
| S. LYONS | | | |

Rev: 10
Date: 07/07/1999